UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,835	07/10/2003	Martin McAfee	016295.1342 (DC-04829)	2696

7590 03/06/2006

Ann C. Livingston
Baker Botts L.L.P.
One Shell Plaza
910 Louisiana
Houston, TX 77002-4995

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,835	MCAFEE ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/10/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to application filed on 10 July 2003.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 10 July 2003 was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

3. The disclosure is objected to because of the following informalities:

4. In specifications, replace "Figure 3" in line 15, on page 7 with ---FIGURE 2--- as figure 2 describes the stated components.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1 – 20, are rejected under 35 U.S.C. 103(a) as being unpatentable over Green et al. [hereinafter as Green], US Patent 6,496,881 B1, and further in view of Poisner, US 2002/0087907 A1.

6. As per claims 1, 7, and 14, Green discloses a multiprocessing system [an information handling system] method for disabling processor by discontinuing supplying the power by voltage regulator module [VRM] response to receiving the control signal from the control logic [64] and isolating the problematic processor upon system reset, having multiple nodes [fig. 2], each having one or more processors [CPU 31-38], and a plurality of voltage regulator modules [VRM41-VRM48] associated therewith, a temperature monitor [64 control logic] such that it may receive a thermal trip [control] signal from each processor [CPU], a voltage control module [VRM] to each node [VRM 41-48] and is operable to deliver voltage [to power] to all processors [CPUs] of the associated node when an enable signal [VRM Enable] is on and to shut off power to all processors of the node when the enable signal [VRM Enable] is off, enable signal [VRM Enable] remains off during a system reset; and deliver a system power signal to a system reset controller; and resetting the system, such that all nodes other than the node containing the overheated processor regain power [col. 3, lines 11 – 45, col. 4, lines 40 – 51, col. 5, lines 1 – 67, col. 6, lines 1 – 5, col. 7, lines 10 – 67, col. 8, lines 1 – 64].

However, Green's control logic with enabling and disabling of control signal [VRM Enable] for supplying and discontinuing power supply does not explicitly disclose

receiving a thermal trip signal from over heated processor and enable and disable control signal to the voltage control module of the node containing the overheated processor.

Poisner discloses an apparatus and method for recovering from an overheated microprocessor in a computer system [100] including processor [110] having an internal thermal [temperature] sensor, processor [110] asserts [enables] a thermal trip signal [111] when the internal temperature of the processor [110] exceeds a maximum acceptable limit indicating that the processor is in an overheated condition and thermal trip signal [111] is delivered to system logic device [120] which includes a reset unit and power management unit [130] and responsive to receiving an assertion of the thermal trip signal [111] power management unit asserts power off signal [131] to voltage regulator module [VRM] and in response to power off signal [131] the voltage regulator module [150 VRM] ceases to deliver the power [abstract, para 0007 – 0009, and 0015 on page 1 – 2, fig. 1 - 2].

It would have been obvious to one of ordinary skill in art, having the teachings of Green and Poisner before him at the time of invention was made, to modify the multiprocessor system and method of disabling a processor as disclosed by Green to include a processor [110] having an internal thermal [temperature] sensor, asserting [enables] a thermal trip signal [111] when the internal temperature of the processor [110] exceeds a maximum acceptable limit indicating that the processor is in an overheated condition and thermal trip signal [111] is delivered to system logic device [120] with power management unit [130] to receive an assertion of the thermal trip

signal [111] and asserts power off signal [131] to voltage regulator module [VRM] ceases to deliver the power to processor as taught by Poisner [abstract, para 0007 – 0009 on page 1, fig. 1 – 2], in order to obtain multiprocessor system (i) to recover from overheated processor, (ii) able to deliver failure message by indicating a status bit to the computer basic input output system [BIOS] software for the system reset, and (iii) power management [130] will cease to reset the processor and will keep the power off signal [131] asserted [para 0007, 00014 – 0015 on page 1 – 2].

7. As to claims 2 – 3, 8, and 15 – 16, Poisner teaches asserting a thermal trip signal [111] when an internal temperature of processor exceeds a maximum acceptable limit including an internal thermal [temperature] sensor which inherently teaches programmable logic device [para 0008 on page 1].

8. As to claim 4, Green discloses system reset, which inherently includes that the resetting is performed by system control unit [fig. 3].

9. As to claims 5, 11 – 12, and 19, Poisner teaches delivering step by asserting a thermal trip signal when an internal temperature of processor at node exceeds acceptable limit indicating an overheated processor [para 0008 on page 1].

10. As to claim 6, Green discloses a multiprocessor system, which inherently teaches to perform automatic resetting in response to system power signal [col. 3, lines 66 – 67, fig. 1].

11. As to claim 9, Poisner discloses a processor [110] with an internal thermal sensor including turns on [asserting] or off [deasserting] the enable signal [VRM Enable] via

connection to a system control unit [120 system logic device] [para 0008 – 0009 on page 1, fig. 1].

12. As to claims 10, and 18, Poisner discloses a processor [110] with an internal thermal sensor includes triggering the reset by asserting a thermal trip signal to logic device, which includes a system reset unit [140] [para 0009 on page 1, fig. 1].

13. As to claim 17, Poisner discloses a processor [110] with an internal thermal sensor including turns on [asserting] or off [deasserting] the enable signal [VRM Enable] via connection to the voltage control unit [150 VRM] through a system control unit [120 system logic device] [para 0008 – 0009 on page 1, fig. 1].

14. As to claims 13, and 20, Poisner teaches a processor with a thermal [temperature] sensor, which inherently teaches operation responsive to a PROHOT signal [as applicant has admitted in background of disclosure in lines 2 – 23 on page 2].

15. **Examiner's note**: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

16. **Prior Art not relied upon**: Please refer to the references listed in attached PTO-892, which, are not relied upon for claim rejection since these references are relevant to the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 571-272-3675. The examiner can normally be reached on 6:45 am - 5:15 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on 571-272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Nitin C. Patel
March 1, 2006